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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/532,411	03/22/2000	Kevin X. Zhang	42390.P8265	8316

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EXAMINER	
DINH, NGOC V	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/532,411	ZHANG, KEVIN X.	
	Examiner	Art Unit	
	NGOC V. DINH	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,7,16-20,24 and 25* is/are rejected.

7)☐ Claim(s) *4,5,8-15 and 21-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/18/03 2/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

INFORMATION DISCLOSURE STATEMENT

1. The Applicant's submission of the IDS filed 08/11/03, 02/10/03 have been considered. As required by M.P.E.P. 609 C(2), a copy of the PTOL-1449 is attached to the instant office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-3, 6-7, 25 are rejected under 35 U.S.C.102 (e) as being anticipated by Takase PN 6762964.

Per claim 1:

Takase teaches:

An apparatus for accessing data in a memory [fig. 1], the apparatus comprising:

a bit vector replacement circuit [replacement control, 8, fig. 4] to receive a first bit vector and a control signal and to substitute a constant bit vector for the first bit vector, in response to the control signal being in a first state, to produce a second bit vector [col. 1, lines 25-30; col. 2, lines 60-65; col. 6, lines 16-50];

a pre-decoder [506, fig. 4]coupled with the bit vector replacement circuit to receive a plurality of bit vectors including the second bit vector, to combine subsequences from the plurality of bit vectors to identify possible wordline subsequences corresponding to the plurality of bit vectors, and to activate a subsequence indicator for an identified possible wordline subsequence [col. 3, lines 20-29; decoder, fig 5; col. 4, lines 61-65; col. 5, lines 1-25] and

a wordline decoder [row/column decoder; fig. 1] coupled with the pre-decoder to combine activated subsequence indicators to identify a unique wordline corresponding to the plurality of bit vectors [col. 4, lines 48-60; col. 6, lines 35-65].

Per claim 2:

Inherently, takase teaches: the plurality of bit vectors correspond to an address represented in carry-sum redundant form. This is because in order to access a memory cell in a memory device, a row and a column address are provided to the arithmetic operation circuit. The arithmetic operation comprises: The multiplication, adding, subtracting operations. The multiplication operation may be thought of as having two parts. The first part is dedicated to the generation of partial products and the second one collects and sums the partial products to obtain the final result. when the partial products from one multiplier operation are first added, the result is initially in a redundant format, such as carry-sum. That it, the result takes the form of two rows of binary information, a carry row and a sum row.

Per claim 3:

Inherently, Takase teaches: the plurality of bit vectors comprise: a carry bit vector including a carry bit corresponding to a binary digit of the address [row address] and a sum bit vector including a sum bit corresponding to a binary digit of the address [column address. This is because in the arithmetic operation, the multiplication operation may be thought of as having two parts and two operands [row and column]: the first part [carry bit associated with row address] is dedicated to the generation of partial products and the second one [sum bit associated with column address] collects and sums the partial products to obtain the final result.

Per claim 6:

the plurality of bit vectors correspond to an address represented in sign-digit redundant form [col. 1, lines 35-45].

Per claim 7:

Inherently, Takase teaches: the plurality of bit vectors comprise: a sign bit vector including a sign bit corresponding to a binary digit of the address; and a magnitude bit

vector including a magnitude bit corresponding to a binary digit of the address. This is because it is well-known in the art that a scalar vector is represented in a mathematic form of two part: the sign bit of the vector [first bit reserved for positive/negative sign] and the magnitude bit indicates the size of the vector.

Per claim 25:

a method of accessing data in a first storage, the method comprising:
copying a plurality of storage locations from a second storage into a plurality of lines of the first storage [storing mapping information indicative of the relationship between the storage circuits and the redundancy cell arrays, col. 3, lines 1-25] by asserting corresponding line signals; receiving an access request including a first bit vector [number of row, col. 4, lines 38-45, row direction, fig. 1], a second bit vector [number of column, col. 4, lines 35-45, ; column direction, fig.1] and a control signal; setting the second bit vector equal to a constant bit vector if the control signal is in a first state [col. 5, lines 49-60]; identifying a line corresponding to the combined first bit vector and second bit vector; asserting the identified line signal, and accessing the line of the first storage corresponding to the asserted line signal [col. 3, lines 49-65; col. 6, lines 17-35].

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 24 are rejected under 35 U.S.C.102 (b) as being anticipated by Auslander et al. PN 5835928.

Per claim 24:

Auslander teaches: a cache memory system [col. 4, lines 49-57] comprising: a plurality of lines for storing copies of memory storage locations having corresponding addresses [col. 6, lines 33-40]; means for decoding an address to access a line of the cache memory system [col. 6, lines 53-65; col. 7, lines 30-40] responsive to an access request that

includes an address represented in an redundant form [multi-bit binary address, col. 5, lines 5-18]; and

Means for decoding an address to access a line of the cache memory system responsive to an access request that includes an address represented in unsigned binary form [col. 6, lines 33-60].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 16-18 are rejected under 35 U.S.C 103(a) as being unpatentable over Takase.

Per claim 16:

Takase teaches the claimed limitation as noted above.

takase does not teach a cache coupled with the wordline decoder to store a copy of a datum stored in the memory, the copy being stored at a wordline in the cache corresponding to an address in the memory.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include a cache into Tasake computer system in order to reduce latency access. This is because cache is a well-known fast memory device for providing data to processor with minimum access latency.

Per claim 17:

Takase teaches: a processor coupled with the pre-decoder to produce the plurality of bit Vectors [col. 7, lines 50-60].

Per claim 18:

Inherently, Takase teaches:the processor produces one or more of the plurality of bit vectors by adding together addressing components including a base address and an index or a displacement. This is because the host accesses [requesting] data stored in the apparatus through a selector in a virtual address which contains an offset or index or

displacement. The host represents a host real address needs to be accessed to the apparatus. This real address include a base address [data holding location/first value] of the segment of the apparatus holding the CPU-specific data. An offset in the virtual address as mentioned above is added to the base address of the segment of the apparatus holding the CPU-specific data to obtain a linear address. This linear address is used to access the entry in the memory device.

5. Claims 19-20 are rejected under 35 U.S.C 103(a) as being unpatentable over Takase, and in view of Lopez-Aguado et al PN 6317,810.

Per claim 19:

Takase teaches: a digital computing system comprising'.

a die [fig. 1];

a bit vector selection circuit on the die to receive a first bit vector and a control signal, and to select a constant bit vector or the first bit vector responsive to the control signal, and to output the selected bit vector as a second bit vector [col. 1, lines 25-30; col. 2, lines 60-65; col. 6, lines 16-50];

a decoder circuit on the die coupled to the bit vector selection circuit to receive a plurality of bit vectors including the second bit vector and to combine a subsequence from each of the plurality of bit vectors to identify a wordline corresponding to the plurality of bit vectors; a processor on the die coupled with the decoder circuit to produce the plurality of bit vectors; a processor on the die coupled with the decoder circuit to produce the plurality of bit vectors [col. 3, lines 20-29; decoder, fig 5; col. 4, lines 61-65; col. 5, lines 1-25].

Takase does not teaches:

an internal cache on the die, the internal cache coupled with the decoder circuit to store a first datum at the wordline corresponding to the plurality of bit vectors; and

an external cache, not on the die, to store a second datum, the external cache coupled with the die and with the internal cache, to transmit the second datum to the internal cache to be stored on the die.

Lopez-Aguado teache;

an internal cache on the die [cache 14 inside CPU, fig. 1] the internal cache coupled with the decoder circuit to store a first datum at the wordline corresponding to the plurality of bit vectors; and an external cache, not on the die [16, fig. 1] to store a second datum, the external cache coupled with the die and with the internal cache, to transmit the second datum to the internal cache to be stored on the die [col. 2, lines 10-45].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include internal/external cache into Tasake computer system in order to reduce latency access. This is because cache is a well-known fast memory device for providing data to processor with minimum access latency.

Per claim 20:

Inherently Takase teaches: the plurality of bit vectors correspond to an address represented in carl-sum redundanl form and the plurality of bit vectors comprise: a carry bit vector including a carœ bit corresponding to a binary digit of the address; and a sum bit vector including a sum bit corresponding to a binary digit of the address.

The reason of the inherence is provided in claims 2-3 above.

Allowable Subject Matter

6. Claims 4-5, 8-15, 21-23 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Yetter PN 5875121 discloses register selection system and method.

b. Zettler et al. PN 6034902 discloses solid state memory device.

c. Sato PN 5999457 discloses semiconductor integrated circuit.

d. Muranaka et al. PN 6282141 discloses semiconductor memory device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (571) 272-4191. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 (571) 272-2100 for regular communications and (703) 746-7238 for After Final communications.
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

NGOC DINH
Patent Examiner
ART UNIT 2187
May 18, 2005

DONALD SPARKS
SUPERVISORY PATENT EXAMINER